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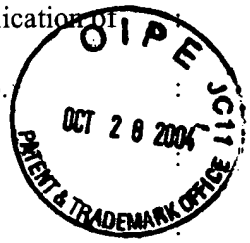
DOCKET NO. 00-BN-051 (STMI01-00051) **PATENT**
Customer No. 30425

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE



In re application of	:	Anthony X. Jarvis, et al
Serial No.	:	09/751,372
Filed	:	December 29, 2000
For	:	SYSTEM AND METHOD FOR EXECUTING VARIABLE LATENCY LOAD OPERATIONS IN A DATA PROCESSOR
Group No.	:	2183
Examiner	:	Barry J. O'Brien

MAIL STOP APPEAL BRIEF - PATENTS
Commissioner for Patents
P.O. Box 1450
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Sir:

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The undersigned hereby certifies that the following documents:

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2) Appeal Brief;
3) Check in the amount of $340.00 for the Appeal Brief filing fee; and
4) Fee Transmittal for FY 2005 (in duplicate).

relating to the above patent application, were deposited as "First Class Mail," with the United States Postal Service, addressed to: MAIL STOP APPEAL BRIEF - PATENTS, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on October 25, 2004.

Date: Oct 25, 2004 Kathy Hamilton
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FEE TRANSMITTAL for FY 2005

Effective 10/01/2004. Patent fees are subject to annual revision.

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) 340.00

Complete if Known	
Application Number	09/751,372
Filing Date	December 29, 2000
First Named Inventor	Anthony X. Jarvis
Examiner Name	Barry J. O'Brien
Art Unit	2183
Attorney Docket No.	00-BN-051 (STMI01-00051)

METHOD OF PAYMENT *(check all that apply)*

☑ Check ☐ Credit card ☐ Money Order ☐ Other ☐ None

☑ Deposit Account:

Deposit Account Number: 05-0208

Deposit Account Name: Davis Munck, P.C.

The Director is authorized to: *(check all that apply)*

☐ Charge fee(s) indicated below ☑ Credit any overpayments

☑ Charge any additional fee(s) or any underpayment of fee(s)

☐ Charge fee(s) indicated below, **except for the filing fee** to the above-identified deposit account.

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1001	790	2001	395	Utility filing fee	
1002	350	2002	175	Design filing fee	
1003	550	2003	275	Plant filing fee	
1004	790	2004	395	Reissue filing fee	
1005	160	2005	80	Provisional filing fee	

SUBTOTAL (1) ($) 0

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

	Extra Claims		Fee from below		Fee Paid
Total Claims		-20** =		X	=
Independent Claims		- 3** =		X	=
Multiple Dependent					=

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description
1202	18	2202	9	Claims in excess of 20
1201	88	2201	44	Independent claims in excess of 3
1203	300	2203	150	Multiple dependent claim, if not paid
1204	88	2204	44	** Reissue independent claims over original patent
1205	18	2205	9	** Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($) 0

***or number previously paid, if greater; For Reissues, see above*

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Large Entity Fee ($)	Small Entity Fee Code	Small Entity Fee ($)	Fee Description	Fee Paid
1051	130	2051	65	Surcharge - late filing fee or oath	
1052	50	2052	25	Surcharge - late provisional filing fee or cover sheet	
1053	130	1053	130	Non-English specification	
1812	2,520	1812	2,520	For filing a request for *ex parte* reexamination	
1804	920*	1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	1805	1,840*	Requesting publication of SIR after Examiner action	
1251	110	2251	55	Extension for reply within first month	
1252	430	2252	215	Extension for reply within second month	
1253	980	2253	490	Extension for reply within third month	
1254	1,530	2254	765	Extension for reply within fourth month	
1255	2,080	2255	1,040	Extension for reply within fifth month	
1401	340	2401	170	Notice of Appeal	
1402	340	2402	170	Filing a brief in support of an appeal	340.00
1403	300	2403	150	Request for oral hearing	
1451	1,510	1451	1,510	Petition to institute a public use proceeding	
1452	110	2452	55	Petition to revive - unavoidable	
1453	1,370	2453	685	Petition to revive - unintentional	
1501	1,370	2501	685	Utility issue fee (or reissue)	
1502	490	2502	245	Design issue fee	
1503	660	2503	330	Plant issue fee	
1460	130	1460	130	Petitions to the Commissioner	
1807	50	1807	50	Processing fee under 37 CFR 1.17(q)	
1806	180	1806	180	Submission of Information Disclosure Stmt	
8021	40	8021	40	Recording each patent assignment per property (times number of properties)	
1809	790	2809	395	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	790	2810	395	For each additional invention to be examined (37 CFR 1.129(b))	
1801	790	2801	395	Request for Continued Examination (RCE)	
1802	900	1802	900	Request for expedited examination of a design application	

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid

SUBTOTAL (3) ($) 340.00

SUBMITTED BY				(Complete *(if applicable)*)	
Name (Print/Type)	William A. Munck	*Registration No. (Attorney/Agent)*	39,308	*Telephone*	972-628-3600
Signature				*Date*	Oct. 25, 2004

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DOCKET NO.: 00-BN-051 (STMI01-00051) **PATENT**
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10/29/2004 HALI11 00000038 09751372
01 FC:1402 340.00 OP

APPEAL BRIEF

The Appellants have appealed to the Board of Patent Appeals and Interferences from the decision of the Examiner dated April 22, 2004, finally rejecting Claims 1-22. The Appellants filed a Notice of Appeal on August 23, 2004, which was received by the U.S. Patent and Trademark Office on August 26, 2004. The Appellants respectfully submit this brief on appeal with the statutory fee of $340.00.

REAL PARTY IN INTEREST

This application is currently owned by STMicroelectronics, Inc. as indicated by:

an assignment recorded on May 7, 2001 in the Assignment Records of the United States Patent and Trademark Office at Reel 011769, Frame 0373;

an assignment recorded on August 2, 2001 in the Assignment Records of the United States Patent and Trademark Office at Reel 012044, Frame 0363; and

an assignment recorded on January 3, 2002 in the Assignment Records of the United States Patent and Trademark Office at Reel 012415, Frame 0370.

RELATED APPEALS AND INTERFERENCES

There are no known appeals or interferences that will directly affect, be directly affected by, or have a bearing on the Board's decision in this pending appeal.

STATUS OF CLAIMS

Claims 1-22 have been rejected pursuant to a final Office Action dated April 22, 2004. Claims 1-22 are presented for appeal. A copy of the claims is provided in Appendix A.

STATUS OF AMENDMENTS

No amendments were filed and refused entry after issuance of the final Office Action dated April 22, 2004.

SUMMARY OF CLAIMED SUBJECT MATTER

Regarding Claim 1, a data processor 100 includes an instruction pipeline 400. (*Application, Page 24, Lines 20-22*). The pipeline 400 includes N processing stages 401-407. (*Application, Page 25, Lines 1-4*). Each of the processing stages 401-407 performs an execution step associated with a pending instruction being executed by the pipeline 400. (*Application, Page 25, Line 5 – Page 28, Line 8*). A data cache 330 is capable of storing data values used by the pending instruction. (*Application, Page 11, Lines 11-12; Page 28, Lines 13-19*). A plurality of registers 310 is capable of receiving the data values from the data cache 330. (*Application, Page 11, Lines 13-14; Page 27, Line 22 – Page 28, Line 2*). A load store unit 325 is capable of transferring a first data value from the data cache 330 to a target register during execution of a load operation. (*Application, Page 29, Line 8 – Page 30, Line 2*). A shifter circuit 535 is capable of shifting, sign extending, or zero extending the first data value prior to loading the first data value into the target register. (*Application, Page 29, Lines 17-22*). Bypass circuitry 530 is capable of transferring the first data value from the data cache 330 directly to the target register without processing the first data value in the shifter circuit 535. (*Application, Page 28, Line 20 – Page 29, Line 7*).

Regarding Claim 10, a method 600 for performing load operations in a data processor 100 is provided. (*Application, Page 29, Lines 8-10*). The method 600 includes determining if a pending instruction in an N-stage execution pipeline 400 is one of a load word operation, a load half-word operation, and a load byte operation. (*Application, Page 29, Lines 13-22*). If the pending instruction is a load half-word operation or a load byte operation, the method 600 includes transferring a first data value from a data cache 330 to a shifter circuit 535 and shifting the first data value prior to

loading the first data value into a target register. (*Application, Page 29, Lines 10-13 and 17-22*). If the pending instruction is a load word operation, the method 600 includes transferring the first data value from the data cache 330 directly to the target register without processing the first data value in the shifter circuit 535. (*Application, Page 29, Lines 13-17*).

Regarding Claim 14, a processing system 10 includes a data processor 100, a memory 130, and a plurality of memory-mapped peripheral circuits 111-114 for performing selected functions. (*Application, Page 17, Lines 9-17*). The data processor 400 includes an instruction execution pipeline 400 having N processing stages 401-407, each of which is capable of performing an execution step associated with a pending instruction being executed. (*Application, Page 24, Line 20 – Page 28, Line 8*). The data processor 400 also includes a data cache 330 capable of storing data values used by the pending instruction. (*Application, Page 11, Lines 11-12; Page 28, Lines 13-19*). The data processor 400 further includes a plurality of registers 310 capable of receiving the data values from the data cache 330. (*Application, Page 11, Lines 13-14; Page 27, Line 22 – Page 28, Line 2*). The data processor 400 also includes a load store unit 325 capable of transferring a first data value from the data cache 330 to a target register during execution of a load operation. (*Application, Page 29, Line 8 – Page 30, Line 2*). The data processor 400 further includes a shifter circuit 535 capable of shifting, sign extending, or zero extending the first data value prior to loading the first data value into the target register. (*Application, Page 29, Lines 17-22*). In addition, the data processor 400 includes bypass circuitry 530 capable of transferring the first data value from the data cache 330 directly to the target register without processing the first data value in the shifter circuit 535. (*Application, Page 28, Line 20 – Page 29, Line 7*).

GROUNDS OF REJECTION

1. Claims 1-22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,761,469 in view of U.S. Patent No. 6,412,061.

ARGUMENT

I. GROUND OF REJECTION #1 (§ 103 REJECTION)

The rejection of Claims 1-22 under 35 U.S.C. § 103(a) is improper and should be withdrawn.

A. OVERVIEW

Claims 1-22 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,761,469 to Greenley et al. ("*Greenley*") in view of U.S. Patent No. 6,412,061 to Dye ("*Dye*").

A copy of *Greenley* is provided in Appendix B. A copy of *Dye* is provided in Appendix C.

B. STANDARD

In *ex parte* examination of patent applications, the Patent Office bears the burden of establishing a *prima facie* case of obviousness. (*MPEP § 2142; In re Fritch, 972 F.2d 1260, 1262, 23 U.S.P.Q.2d 1780, 1783 (Fed. Cir. 1992)*). The initial burden of establishing a *prima facie* basis to deny patentability to a claimed invention is always upon the Patent Office. (*MPEP § 2142; In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Piasecki, 745 F.2d 1468, 1472, 223 U.S.P.Q. 785, 788 (Fed. Cir. 1984)*). Only when a *prima facie* case of obviousness is established does the burden shift to the Appellants to produce evidence of nonobviousness.

(*MPEP § 2142; In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Rijckaert, 9 F.3d 1531, 1532, 28 U.S.P.Q.2d 1955, 1956 (Fed. Cir. 1993)*). If the Patent Office does not produce a *prima facie* case of unpatentability, then without more the Appellants are entitled to grant of a patent. (*In re Oetiker, 977 F.2d 1443, 1445, 24 U.S.P.Q.2d 1443, 1444 (Fed. Cir. 1992); In re Grabiak, 769 F.2d 729, 733, 226 U.S.P.Q. 870, 873 (Fed. Cir. 1985)*).

A *prima facie* case of obviousness is established when the teachings of the prior art itself suggest the claimed subject matter to a person of ordinary skill in the art. (*In re Bell, 991 F.2d 781, 783, 26 U.S.P.Q.2d 1529, 1531 (Fed. Cir. 1993)*). To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed invention and the reasonable expectation of success must both be found in the prior art, and not based on Appellants' disclosure. (*MPEP § 2142*).

C. THE *GREENLEY* REFERENCE

Greenley recites a method and apparatus for improving the performance of pipelined processors. (*Abstract*). The apparatus of *Greenley* includes a data cache 180, an aligning unit 170, and a sign extension unit 160. (*Figure 1*). The aligning unit 170 aligns data retrieved from the data cache 180, and the sign extension unit 160 extends the sign of the retrieved data. (*Col. 2, Lines 32-*

54). In particular, the aligning unit 170 right justifies the data retrieved from the data cache 180, and the sign extension unit 160 fills unoccupied bits with sign information. (*Col. 2, Lines 36-50*).

D. THE *DYE* REFERENCE

Dye recites a method for adjusting a processor pipeline and bypassing unnecessary stages. (*Abstract*). For each instruction to be executed, the number of stages needed to execute the instruction is determined. (*Abstract*). Unnecessary stages of the processor pipeline are bypassed. (*Abstract*).

E. CLAIMS 1-22

Claim 1 recites a data processor, which includes:

> an instruction execution pipeline comprising N processing stages, each of said N processing stages capable of performing one of a plurality of execution steps associated with a pending instruction being executed by said instruction execution pipeline;
>
> a data cache capable of storing data values used by said pending instruction;
>
> a plurality of registers capable of receiving said data values from said data cache;
>
> a load store unit capable of transferring a first one of said data values from said data cache to a target one of said plurality of registers during execution of a load operation;
>
> a shifter circuit associated with said load store unit capable of one of a) shifting, b) sign extending, or c) zero extending said first data value prior to loading said first data value into said target register; and
>
> bypass circuitry associated with said load store unit capable of transferring said first data value from said data cache directly to said target register without processing said first data value in said shifter circuit.

The Examiner acknowledges that *Greenley* fails to disclose the use of "bypass circuitry" that is capable of "transferring [a] first data value from [a] data cache directly to [a] target register without processing [the] first data value in [a] shifter circuit" as recited in Claim 1. (*04/22/04 Office Action, Page 4, Paragraph 8*). The Examiner then asserts that *Dye* discloses these elements of Claim 1 and that it would be obvious to combine *Dye* with *Greenley*. (*04/22/04 Office Action, Page 4, Paragraph 9*).

The Examiner has failed to establish a *prima facie* case of obviousness against Claim 1 using the proposed *Greenley-Dye* combination. In particular, the Examiner has failed to establish that a person skilled in the art would modify *Greenley* as proposed by the Examiner.

The Examiner asserts that a person skilled in the art would be motivated to modify *Greenley* because "the sign extension and alignment units" of *Greenley* are not needed "when fetched data occupies the entire register." (*04/22/004 Office Action, Page 4, Paragraph 9*). Based on this, the Examiner asserts that a person skilled in the art would be motivated to "include a bypass path around the unused sign extension and aligning units because doing so would reduce the latency required to load data." (*04/22/004 Office Action, Page 4, Paragraph 9*).

The Examiner's position is based on the assumption that the sign extension and aligning units of *Greenley* are not needed when "fetched data occupies the entire register." For example, double words (64-bit words) may be retrieved and processed by a 64-bit wide aligning unit. (*Col. 2, Lines 19-20; Col. 8, Lines 59-60*).

The Examiner's position is contradicted by the express recitations of *Greenley*. Regarding the aligning unit, *Greenley* specifically recites that load access to a data cache "must" insure that the

accessed data is aligned. (*Col. 2, Lines 20-25*). *Greenley* also specifically recites that "double words" are "similarly aligned by the aligning unit." Regarding the sign extension unit, *Greenley* specifically recites that "double-words" are "similarly sign extended" by "the sign extension unit." (*Col. 2, Lines 60-61*).

These portions of *Greenley* specifically recite that the aligning unit must examine retrieved data even when a double word is retrieved from the data cache. The aligning unit must examine the retrieved data because the data may not be physically stored in consecutive locations in the data cache. (*Col. 2, Lines 19-25*). Based on this, the aligning unit of *Greenley* cannot be skipped when double words are retrieved as asserted by the Examiner. Similarly, these portions of *Greenley* specifically show that the sign extension unit processes the retrieved data even when a double word is retrieved from the data cache.

The Examiner relies on the statement in *Greenley* that "needed data *may* not be physically stored consecutively in [the] data cache" at column 2, lines 20-21 (italics added). (*08/31/04 Interview Summary, Page 3, First paragraph*). The Examiner also asserts that *Greenley* is "silent as to what happens when data that is already aligned is in the data cache." (*08/31/04 Interview Summary, Page 3, First paragraph*). Based on this, the Examiner asserts that *Greenley* does not teach away from using the bypass mechanism of *Dye*. (*08/31/04 Interview Summary, Page 3, First paragraph*). However, the only component in *Greenley* that determines whether data needs alignment is the aligning unit. As a result, the data from the data cache of *Greenley* must be provided to the aligning unit of *Greenley*, even if the data is already aligned. As a result, the aligning unit cannot be skipped even if data is physically stored consecutively in a data cache.

The aligning and sign extension units of *Greenley* must receive and process the retrieved data even if the retrieved data represents a double word and even if the retrieved data is aligned. As a result, the Examiner's assertion that these units may be bypassed is incorrect. Also, because these units may not be skipped, a person skilled in the art would not be motivated to include bypass circuitry for bypassing these units as asserted by the Examiner.

For these reasons, the Examiner has not shown that a person skilled in the art would modify *Greenley* to include "bypass circuitry" capable of "transferring [a] first data value from [a] data cache directly to [a] target register without processing [the] first data value in [a] shifter circuit" as recited in Claim 1. As a result, the Examiner has not established a *prima facie* case of obviousness against Claim 1 (and its dependent claims).

Greenley and *Dye* both fail to disclose, teach, or suggest transferring a data value to a "shifter circuit" in response to a determination that a pending instruction is a "load half-word operation" or a "load byte operation" as recited in Claim 10. *Greenley* and *Dye* also both fail to disclose, teach, or suggest transferring a data value directly to a "target register" without processing the first data value in the "shifter circuit" in response to a determination that a pending instruction is a "load word operation" as recited in Claim 10. As a result, the Examiner has not established a *prima facie* case of obviousness against Claim 10 (and its dependent claims).

Claim 14 recites elements that are analogous to the elements of Claim 1 discussed above. As a result, the Examiner has not established a *prima facie* case of obviousness against Claim 14 (and its dependent claims).

For these reasons, the Examiner has not established a *prima facie* case of obviousness against

Claims 1-22. Accordingly, the Appellants respectfully request that the final rejection of Claims 1-22 be withdrawn and that Claims 1-22 be passed to allowance.

SUMMARY

The Appellants have demonstrated that the present invention as claimed is clearly distinguishable over the prior art cited of record. Therefore, the Appellants respectfully request the Board of Patent Appeals and Interferences to reverse the final rejection of the Examiner and instruct the Examiner to issue a notice of allowance of all claims.

The Appellants have enclosed a check in the amount of $340.00 to cover the cost of this Appeal Brief. The Appellants do not believe that any additional fees are due. However, the Commissioner is hereby authorized to charge any additional fees (including any extension of time fees) or credit any overpayments to Davis Munck Deposit Account No. 50-0208.

Respectfully submitted,

DAVIS MUNCK, P.C.

Date: Oct. 25, 2004

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APPENDIX A

PENDING CLAIMS

1. A data processor comprising:

an instruction execution pipeline comprising N processing stages, each of said N processing stages capable of performing one of a plurality of execution steps associated with a pending instruction being executed by said instruction execution pipeline;

a data cache capable of storing data values used by said pending instruction;

a plurality of registers capable of receiving said data values from said data cache;

a load store unit capable of transferring a first one of said data values from said data cache to a target one of said plurality of registers during execution of a load operation;

a shifter circuit associated with said load store unit capable of one of a) shifting, b) sign extending, or c) zero extending said first data value prior to loading said first data value into said target register; and

bypass circuitry associated with said load store unit capable of transferring said first data value from said data cache directly to said target register without processing said first data value in said shifter circuit.

2. The data processor as set forth in Claim 1 wherein said bypass circuitry transfers said first data value from said data cache directly to said target register during a load word operation.

3. The data processor as set forth in Claim 2 wherein said bypass circuitry transfers said first data value from said data cache directly to said target register at the end of two machine cycles.

4. The data processor as set forth in Claim 1 wherein said shifter circuit one of a) shifts, b) sign extends, or c) zero extends said first data value prior to loading said first data value into said target register during a load half-word operation.

5. The data processor as set forth in Claim 4 wherein said shifter circuit loads said shifted first data value into said target register at the end of three machine cycles.

6. The data processor as set forth in Claim 1 wherein said shifter circuit one of a) shifts, b) sign extends, or c) zero extends said first data value prior to loading said first data value into said target register during a load byte operation.

7. The data processor as set forth in Claim 6 wherein said shifter circuit loads said shifted first data value into said target register at the end of three machine cycles.

8. The data processor as set forth in Claim 1 wherein said bypass circuitry comprises a multiplexer having a first input channel coupled to a data output of said data cache.

9. The data processor as set forth in Claim 8 wherein said multiplexer has a second input channel coupled to an output of said shifter circuit.

10. A method of loading a first data value from a data cache into a target register of a plurality of registers, the method comprising the steps of:

determining if a pending instruction in an N-stage execution pipeline is one of a load word operation, a load half-word operation, and a load byte operation;

in response to a determination that the pending instruction is a load half-word operation, transferring the first data value from the data cache to a shifter circuit and shifting the first data value prior to loading the first data value into the target register;

in response to a determination that the pending instruction is a load byte operation, transferring the first data value from the data cache to the shifter circuit and shifting the first data value prior to loading the first data value into the target register; and

in response to a determination that the pending instruction is a load word operation, transferring the first data value from the data cache directly to the target register without processing the first data value in the shifter circuit.

11. The method as set forth in Claim 10 wherein the step of transferring the first data value requires two machine cycles during a load word operation.

12. The method as set forth in Claim 10 wherein the step of transferring the first data value requires three machine cycles during a load half-word operation.

13. The method as set forth in Claim 10 wherein the step of transferring the first data value requires three machine cycles during a load byte operation.

14. A processing system comprising:

a data processor;

a memory coupled to said data processor;

a plurality of memory-mapped peripheral circuits coupled to said data processor for performing selected functions in association with said data processor, wherein said data processor comprises:

an instruction execution pipeline comprising N processing stages, each of said N processing stages capable of performing one of a plurality of execution steps associated with a pending instruction being executed by said instruction execution pipeline;

a data cache capable of storing data values used by said pending instruction;

a plurality of registers capable of receiving said data values from said data cache;

a load store unit capable of transferring a first one of said data values from said data cache to a target one of said plurality of registers during execution of a load operation;

a shifter circuit associated with said load store unit capable of one of a) shifting, b) sign extending, or c) zero extending said first data value prior to loading said first data value into said target register; and

bypass circuitry associated with said load store unit capable of transferring said first data value from said data cache directly to said target register without processing said first data value in said shifter circuit.

15. The processing system as set forth in Claim 14 wherein said bypass circuitry transfers said first data value from said data cache directly to said target register during a load word operation.

16. The processing system as set forth in Claim 15 wherein said bypass circuitry transfers said first data value from said data cache directly to said target register at the end of two machine cycles.

17. The processing system as set forth in Claim 14 wherein said shifter circuit one of a) shifts, b) sign extends, or c) zero extends said first data value prior to loading said first data value into said target register during a load half-word operation.

18. The processing system as set forth in Claim 17 wherein said shifter circuit loads said shifted first data value into said target register at the end of three machine cycles.

19. The processing system as set forth in Claim 14 wherein said shifter circuit one of a) shifts, b) sign extends, or c) zero extends said first data value prior to loading said first data value into said target register during a load byte operation.

20. The processing system as set forth in Claim 19 wherein said shifter circuit loads said shifted first data value into said target register at the end of three machine cycles.

21. The processing system as set forth in Claim 14 wherein said bypass circuitry comprises a multiplexer having a first input channel coupled to a data output of said data cache.

22. The processing system as set forth in Claim 21 wherein said multiplexer has a second input channel coupled to an output of said shifter circuit.

APPENDIX B

***Greenley* Reference**

U.S. Patent No. 5,761,469

APPENDIX C

***Dye* Reference**

U.S. Patent No. 6,412,061